

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A strained silicon carbon alloy MOSFET structure, comprising:
 - a substrate;
 - a graded SiGe layer on the substrate;
 - a relaxed buffer layer on the graded SiGe layer;
 - a strained silicon carbon alloy layer on the relaxed buffer layer acting as a channel;
 - a gate dielectric layer on the strained silicon carbon alloy layer;
 - a polysilicon gate electrode on the gate dielectric layer; and
 - a source region and a drain region on the substrate opposite and adjacent to the polysilicon gate electrode.
2. (Original) The structure of claim 1, wherein the relaxed buffer layer comprises Si-Ge-C alloy, Si, Ge or other combinations of at least two semiconductor materials.
3. (Original) The structure of claim 1, wherein the gate dielectric layer comprises HfO₂, Si₃N₄, Al₂O₃, or any high dielectric constant (high k) dielectric material.
4. (Original) The structure of claim 1, wherein the MOSFET is a NMOS or PMOS.
5. (Currently Amended) The structure of claim 1, wherein the gate electrode dielectric layer comprises Al, Pt, TaN, TiN, or any metal gate electrode dielectric.

6. (Currently Amended) The structure of claim 1, wherein the gate electrode polysilicon layer comprises polysilicon and poly-SiGe.

7. (Currently Amended) The structure of claim 5, wherein the gate electrode polysilicon layer comprises n-type or p-type dopants.

8. (Original) The structure of claim 1, wherein the substrate comprises n-type and p-type doped Ge, III-V group semiconductor, or silicon-on-insulator (SOI).

9. (Withdrawn - Currently Amended) A method of strained silicon carbon alloy MOSFET fabrication, comprising the steps of:

forming a graded SiGe layer on a substrate;

forming a relaxed buffer layer on the graded SiGe layer;

forming a strained silicon carbon alloy layer on the relaxed buffer layer acting as a channel;

forming an gate dielectric layer on the strained silicon carbon alloy layer;

forming a gate polysilicon layer on the gate dielectric layer;

etching the gate dielectric layer and the gate polysilicon layer to form a polysilicon gate electrode with a sidewall spacer; and

forming a source/drain region and a drain region on the substrate opposite and adjacent to the polysilicon gate electrode.

10. (Withdrawn) The method of claim 9, wherein the relaxed buffer layer comprises Si-Ge-C alloy, Si, Ge or other combinations of at least two semiconductor materials.

11. (Withdrawn) The method of claim 9, wherein the gate dielectric layer comprises HfO₂, Si₃N₄, Al₂O₃, or any high dielectric constant (high k) dielectric material.

12. (Withdrawn) The method of claim 9, wherein the MOSFET is a NMOS or PMOS.

13. (Withdrawn - Currently Amended) The structure of claim 9, wherein the gate electrode ~~dielectric~~ layer comprises Al, Pt, TaN, TiN, or any metal gate electrode ~~dielectric~~.

14. (Withdrawn - Currently Amended) The method of claim 9, wherein the gate electrode ~~polysilicon~~ layer comprises polysilicon and poly-SiGe.

15. (Withdrawn - Currently Amended) The method of claim 14, wherein the gate electrode ~~polysilicon~~ layer comprises n-type or p-type dopants.

16. (Withdrawn) The method of claim 9, wherein the substrate comprises n-type and p-type doped Ge, III-II group semiconductor, or silicon-on-insulator (SOI).